

ABSTRACT

A mixed voltage CMOS process for high reliability and high
5 performance core transistors and input-output transistors
with reduced mask steps. A gate stack (30) is formed over
the silicon substrate (10). Ion implantation is performed
of a first species and a second species to produce the
doping profiles (70, 80, 90, 100) in the input-output
10 transistors.

100 90 80 70 60 50 40 30 20 10 0